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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

#14 Appeal Brief T. Chung 8-18-03

In re Application of:	
Jong-Woo KIM et al.	Confirmation No.: 2621
Application No.: 09/885,527	Group Art Unit: 2871
Filed: June 21, 2001	Examiner: D. Chung
For: LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME	**Mail Stop Appeal Brief Patents**

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APPELLANTS' BRIEF UNDER 37 C.F.R. § 1.192

This brief is in furtherance of the Notice of Appeal, which was filed in the above-identified patent application on June 24, 2003. The fee required under 37 C.F.R. § 1.17(c) is being filed concurrently herewith. This brief is being filed in triplicate.

1. The Real Party In Interest

The real party in interest in this appeal is LG.Philips LCD Co, Ltd. of Seoul, Korea.

2. Related Appeals and Interferences

Appellants are not aware of any other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the appeal.

3. Status of Claims in Application

The status of the claims is as follows:

Claims canceled: none.
Claims pending: 1-28.
Claims allowed: none.
Claims rejected: 1-17.
Claims withdrawn: 18-28.

The claims on appeal are 1-17, which stand rejected under 35 U.S.C. § 103(a).

4. Status of Amendments

All amendments have been entered. Appellants filed a Request for Reconsideration under 37 C.F.R. § 1.116 (Paper No. 11) on May 22, 2003 in response to the Final Office Action (Paper No. 10) dated February 26, 2003. On June 3, 2003, the Examiner issued an Advisory Action (Paper No. 12) which indicated that the Request for Reconsideration under 37 C.F.R. § 1.116 does not place the application in condition for allowance. On June 24, 2003, Appellants filed a Notice of Appeal (Paper No. 13).

5. Summary of the Invention

Appellants' invention relates generally to a method of fabricating an array substrate for an active-matrix liquid crystal display device for reducing fabrication costs and improving fabrication yields. As discussed in Appellants' specification beginning at paragraph [0024] at page 12, and shown in FIGs. 4 to 8B, for example, an array substrate 100 may be fabricated using four masking steps, each shown in FIGs. 5B, 6B, 7B, and 8B, respectively.

A first mask step, as shown in FIG. 5B, includes depositing a metal layer on a substrate 100. Then, the metal layer is patterned using a first mask to form a gate line 102, a gate electrode 101, and a gate pad 106.

A second mask step, as shown in FIG. 6B, includes formation of a data line 120 and a second capacitor electrode 130 by depositing a first insulating layer 200, a second insulating layer 201, an amorphous silicon layer 202a, a doped amorphous silicon layer 202b, and a second metal layer on the substrate 100. Then, the second metal layer is patterned using a second mask to form the data line 120 and the second capacitor electrode 130.

A third mask step, as shown in FIG. 7B, includes depositing an insulating material to cover the second metal layer. Then, the insulating material is patterned using a third mask to form a capacitor contact hole 202 through a passivation layer 122 positioned over the second capacitor electrode 130, and a data pad contact hole 119 formed through the passivation layer 122 positioned over the data pad 124. In addition, during the third mask step, a portion of the amorphous silicon layer 202a is simultaneously etched together with the insulating material.

A fourth mask step, as shown in FIG. 8B, includes depositing a transparent conductive material on the passivation layer 122. Then, the transparent conductive material is subsequently patterned using a fourth mask to form a pixel electrode 118, a gate pad electrode 107, and a data pad electrode 123.

Appellants discovered that by patterning the insulating material to form the passivation layer 122, the capacitor and data pad contact holes 204 and 119, and patterning the amorphous silicon layer using a single mask, a total number of masking steps and masks required to fabricate the array substrate may be reduced.

6. Issues

The following issue is presented on appeal: whether the rejection of claims 1-17 under 35 U.S.C. § 103(a) as being unpatentable over *Park et al.* (US 6,335,276 B1) in view of *Kim* (US 6,225,130 B1) and *Park et al.* (US 6,287,899 B1) should be reversed because (1)

the Office Action fails to establish a *prima facie* case of obviousness of the claimed invention, and (2) none of the applied references, whether taken singly or in combination, would have rendered the claimed invention as a whole obvious at the time of the invention to a person having ordinary skill in the art.

7. Grouping of Claims

In as far as present herein, claims 1-17 stand or fall together.

8. Arguments

(i) Rejections under 35 U.S.C. § 112, first paragraph

No claims are presently rejected under 35 U.S.C. § 112, first paragraph.

(ii) Rejections under 35 U.S.C. § 112, second paragraph

No claims are presently rejected under 35 U.S.C. § 112, second paragraph.

(iii) Rejections under 35 U.S.C. § 102

No claims are presently rejected under 35 U.S.C. § 102.

(iv) Rejections under 35 U.S.C. § 103

Claims 1-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Park et al.* (US 6,335,276 B1) in view of *Kim* (US 6,225,130 B1) and *Park et al.* (US 6,287,899 B1). Appellants respectfully traverse the rejection as being based upon a combination of references that neither teach nor suggest the novel combination of features recited in independent claim 1, and hence dependent claims 2-17.

Summary of *Park et al. ('276)*

Park et al. ('276) discloses a method of manufacturing a thin film transistor array panel for a liquid crystal display for reducing the number of photolithographic steps. As shown in FIGs. 3-5 of *Park et al.('276)*, a pixel electrode 82 is formed to be electrically interconnected between a drain electrode 66 and a conductor pattern 68 for a storage capacitor formed at an edge portion of a pixel region. In addition, *Park et al. ('276)* discloses (col. 8, lines 63-65) that "if a sufficient storage capacitance can be achieved by the overlap of the pixel electrode 82 and the gate line 22, the conductor islands 68 may not be required."

Summary of *Kim*

Kim discloses a method for manufacturing a thin film transistor array panel with a reduced number of photolithographic steps. As shown in FIGs. 1-3 of *Kim*, a pixel electrode 82 is formed on a passivation layer 70 electrically interconnected between a drain electrode 66 and a conductor pattern 68 for a storage capacitor formed in a central portion of a pixel region. In addition, *Kim* discloses (col. 7, lines 23-25) that "[t]he storage electrode 28 may not be provided if the storage capacitance between the pixel electrode 82 and the gate line 22 is sufficient."

Summary of *Park et al. ('899)*

Park et al. ('899) discloses a method for manufacturing a thin film transistor array panel for a liquid crystal display having reduced manufacturing costs and increased productivity. As shown in FIG. 15 of *Park et al. ('899)*, a pixel electrode 87 formed on a passivation layer 70 is electrically connected to a side portion of a drain electrode 66.

A. Claims 1-17 Are Non-Obvious Over The Applied Art

Claim 1

Independent claim 1 recites a method of fabricating a liquid crystal display device including at least steps of "patterning the passivation layer, the active layer, and the insulating layer" and "forming a pixel electrode on the passivation layer such that the pixel electrode electrically contacts an upper surface of the second capacitor electrode through a contact hole formed in the insulating layer."

It is respectfully submitted that *Park et al. ('276)*, *Kim*, and *Park et al. ('899)*, whether taken individually or in combination, fail to teach or suggest Appellants' invention for at least the following reasons.

The Office Action recognizes that *Park et al. ('276)* does not disclose all of the features recited by independent claim 1. *Kim* is relied upon for allegedly teaching "a storage capacitor formed in the middle of the pixel area with the pixel electrode contacting the storage capacitor electrode through contact holes in the insulation layer" to provide motivation to modify *Park et al. ('276)*. Moreover, the Office Action asserts that it would have been obvious "to form the storage capacitor of Kim (U.S. 6,255,130) in the display of Park et al. (U.S. 6,335,276) because it is **a functionally equivalent alternative** to the storage capacitor disclosed by Park et al. (U.S. 6,335,276)" (emphasis added). Appellants respectfully disagree.

M.P.E.P. § 2143.01 instructs that "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill

in the art." Accordingly, since *Kim* does not provide **any** teaching, suggestion, or motivation to combine or modify the teachings of *Park et al. ('276)*, Appellants respectfully assert that the Office Action has not established a *prima facie* case of obviousness. Appellants further assert that dependent claims 2-17 are allowable at least because of their dependence from independent claim 1, as well as the individual features each of dependent claims 2-17 recite.

Appellants further assert that the Office Action does not rely on *Park et al. ('899)* to provide motivation to modify *Park et al. ('276)* and/or *Kim*. Appellants also respectfully assert that *Park et al. ('899)* cannot provide proper motivation to modify *Park et al. ('276)* and/or *Kim*. Moreover, even if the motivation to combine existed (which Appellants deny), the combination of the references does not teach nor suggest the novel combination of features clearly recited in independent claim 1, and hence dependent claims 2-17.

Furthermore, Appellants respectfully submit that dependent claims 2-17 are allowable for all of the reasons discussed above with regard to independent claim 1, from which they depend, as well as the individual features each of dependent claims 2-17 recite.

For the above reasons, Appellants respectfully assert that the rejection under 35 U.S.C. § 103(a) should be withdrawn because *Park et al. ('276)*, *Kim*, and/or *Park et al. ('899)*, whether taken individually or in combination, neither teach nor suggest the novel combination of features clearly recited in independent claim 1, and hence dependent claims 2-17.

(v) Other Rejections

No claims are presently rejected under grounds other than those referred to above.

In view of the foregoing, Appellants respectfully request the reversal of the Examiner's rejections and allowance of the pending claims. If there are any other fees due in connection with the filing of this Appeal Brief, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account No. 50-0310.

Respectfully submitted,

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9. Appendix

1. A method of fabricating a liquid crystal display device, comprising the steps of:

forming a first metal layer on a substrate to form a gate line including a gate electrode, a gate pad, and a first capacitor electrode;

forming an insulating layer, an active layer, and a second metal layer on the substrate;

patterning the second metal layer to form a data line including a data pad, a source electrode, a drain electrode, and a second capacitor electrode;

forming a passivation layer to cover the second metal layer;

forming a photoresist on the passivation layer;

exposing the photoresist using a mask having a light shielding portion, a light transmissive portion, and a semi-transmissive portion;

forming a first photoresist portion, a second photoresist portion, and a third photoresist portion;

patterning the passivation layer, the active layer, and the insulating layer; and

forming a pixel electrode on the passivation layer such that the pixel electrode electrically contacts an upper surface of the second capacitor electrode through a contact hole formed in the insulating layer.

2. The method of fabricating a liquid crystal display device according to Claim 1, wherein the gate line and the data line cross with each other to define a pixel region, and the source electrode and the drain electrode are spaced apart from each other.

3. The method of fabricating a liquid crystal display device according to Claim 1, wherein the step of depositing and patterning a first metal layer includes a first masking step.

4. The method of fabricating a liquid crystal display device according to Claim 1, wherein the step of depositing an insulating layer, an active layer, and a second metal layer includes a second masking step.

5. The method of fabricating a liquid crystal display device according to Claim 4, wherein the step of patterning the second metal layer is included in the second masking step.

6. The method of fabricating a liquid crystal display device according to Claim 1, wherein the steps of forming a passivation layer, forming a photoresist, exposing the photoresist, forming first, second and third photoresist portions, and patterning the passivation layer are included in a third masking step.

7. The method of fabricating a liquid crystal display device according to Claim 6, wherein, in the third masking step, a side portion and upper surfaces of the drain electrode are uncovered, a capacitor contact hole is formed over the second capacitor electrode, and a data pad contact hole is formed over the data pad through the passivation layer, and a gate pad contact hole is formed over the gate pad passing through the insulating layer, the active layer, and the passivation layer.

8. The method of fabricating a liquid crystal display device according to Claim 1, wherein the third photoresist portion has a thickness of 800 to 900 Å.

9. The method of fabricating a liquid crystal display device according to Claim 1, wherein the first metal layer includes at least a first aluminum neodymium (AlNd) material layer and a second molybdenum (Mo) material layer.

10. The method of fabricating a liquid crystal display device according to Claim 1, wherein the insulating layer and the passivation layer include at least an inorganic insulating material.

11. The method of fabricating a liquid crystal display device according to Claim 10, wherein the inorganic insulating material includes at least one material selected from a group consisting of silicon oxide (SiO_2) and silicon nitride (SiN_X).

12. The method of fabricating a liquid crystal display device according to Claim 1, wherein the insulating layer and the passivation layer include at least organic insulating materials.

13. The method of fabricating a liquid crystal display device according to Claim 12, wherein the organic insulating materials include at least one material selected from a group consisting benzocyclobutene (BCB) and an acryl-based resin.

14. The method of fabricating a liquid crystal display device according to Claim 1, wherein a portion of the passivation layer disposed over the data line has a width smaller than a corresponding width of the data line.

15. The method of fabricating a liquid crystal display device according to Claim 1, wherein the light shielding portion of the mask includes at least an opaque metal material having a low reflectivity.

16. The method of fabricating a liquid crystal display device according to Claim 15, wherein the opaque metal includes at least a chromium (Cr) material.

17. The method of fabricating a liquid crystal display device according to Claim 1, wherein the semi-transmissive portion of the mask includes at least a molybdenum silicide (MoSi) material.

18. A liquid crystal display device, comprising:

a substrate;

a first metal layer disposed on the substrate, the first metal layer includes a gate line connected to a gate electrode, and a first capacitor electrode;

an insulating layer covering the first metal layer;

a silicon layer disposed on the insulating layer, a portion of the silicon layer includes an active layer disposed over the gate electrode;

a second metal layer disposed on the silicon layer, the second metal layer includes a data line, a source electrode, a drain electrode, and a second capacitor electrode;

a passivation layer covering the second metal layer, a side edge portion of the drain electrode being exposed from the passivation layer; and

a pixel electrode disposed on the passivation layer, the pixel electrode contacting the side edge portion of the drain electrode.

19. The liquid crystal display device according to claim 18, wherein the source electrode electrically connects with the data line, the drain electrode is spaced apart from the source electrode, the source and drain electrodes are disposed on the active layer, and the second capacitor electrode is disposed over the first capacitor electrode

20. A halftone mask, comprising:

a light shielding portion shielding a photoresist from incident rays of light;

a semi-transmissive portion transmitting at least a portion of the incident rays of light to the photoresist; and

a light transmissive portion transmitting at least all the incident rays of light to the photoresist.

21. The halftone mask according to Claim 20, wherein the light shielding portion includes at least an opaque metal material having a low reflectivity.

22. The halftone mask according to Claim 20, wherein the opaque metal includes at least a chromium (Cr) material.

23. The halftone mask according to Claim 20, wherein the semi-transmissive portion includes at least a molybdenum silicide (MoSi) material.

24. The halftone mask according to Claim 23, wherein the molybdenum silicide (MoSi) material has a transmissivity of 30 to 40 %.

25. The halftone mask according to Claim 20, wherein the light shielding portion includes at least a molybdenum silicide (MoSi) material layer and a chromium (Cr) material layer sequentially disposed on a transparent substrate.

26. A liquid crystal display device, comprising:

a substrate;

a first metal layer disposed on the substrate, the first metal layer includes at least a gate line that is connected to a gate electrode, and a first capacitor electrode, one end of the gate line is electrically connected to a gate pad;

an insulating layer covering the first metal layer;

a gate pad contact hole formed passing through the insulating layer to uncover a portion of the gate pad;

a silicon layer disposed on the insulating layer, a portion of the silicon layer includes an active layer disposed over the gate electrode;

a second metal layer disposed on the silicon layer, the second metal layer includes at least a data line, a source electrode, a drain electrode, a second capacitor electrode, and a data pad;

a passivation layer covering the second metal layer, a side edge portion of the drain electrode being exposed from the passivation layer; and

a pixel electrode disposed on the passivation layer, the pixel electrode contacting the side edge portion of the drain electrode.

27. The liquid crystal display device according to Claim 26, wherein the source electrode electrically connects with the data line, the drain electrode is spaced apart from the source electrode, the source electrode and the drain electrode are disposed on the active layer, the second capacitor electrode is disposed over the first capacitor electrode, and the data pad is connected to first end of the data line.

28. The liquid crystal display device according to Claim 26, wherein a capacitor contact hole and a data pad contact hole are formed passing through the passivation layer uncovering corresponding portions of the second capacitor electrode and data pad.